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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/653,754	09/03/2003	Stephan G. Meier	5500-97500	3663

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EXAMINER	
KIM, DANIEL Y	

ART UNIT	PAPER NUMBER
2185	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/653,754	MEIER ET AL.	
	Examiner	Art Unit	
	Daniel Kim	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *See Continuation Sheet*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :12/30/03, 1/5/04, 3/22/04, 5/27/05, 3/31/06 and 11/16/06 .

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statements (IDS) submitted on 12/30/03, 1/5/04, 3/22/04, 5/27/05, 3/31/06 and 11/16/06 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements are being considered by the examiner.

Concerning the lined-through references on the IDS submitted 12/30/03, the reference 5802594 appears to have a different inventor than that listed on the IDS by applicant, therefore the reference was not considered by examiner. Similarly, the reference 5521306 does not appear to be the intended reference, as the inventor is different from that listed on applicant's IDS and the subject matter does not seem applicable to the application, therefore the reference was not considered by examiner.

Concerning the lined-through reference on the IDS submitted 1/5/04, the reference 2674044 is not in the English language, therefore the reference has not been considered by examiner.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-11, 13-21, 23 and 27-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Tran (US Patent No. 6,016,533).

For claim 1, Tran discloses a way predictor comprising:

a decoder configured to decode an indication of a first address that is to access a cache, the decoder configured to select a set responsive to the indication of the first address (decoder is coupled to the memory locations and storage locations, and is configured to receive and decode addresses, col. 3, lines 24-29);

a memory coupled to the decoder, wherein the memory is configured to output a plurality of values from a set of storage locations in response to the decoder selecting the set, wherein each of the plurality of values corresponds to a different way of the cache (the decoder may be configured to select a subset of way predictions from a selected set based upon a portion of a requested address, col. 3, lines 41-44); and

a circuit coupled to receive the plurality of values and a first value corresponding to the first address, wherein the circuit is configured to generate a way prediction for the cache responsive to the plurality of values and the first value (the cache memory uses portions of the requested address in parallel to reduce way prediction, col. 3, lines 5-7; a first portion of a requested address is used to select a set of way predictions within the plurality of storage locations, col. 3, lines 22-24).

For claim 2, Tran discloses the circuit comprises a plurality of comparators, wherein each comparator of the plurality of comparators is configured to compare a respective one of the plurality of values to the first value, and wherein the circuit is configured to generate the way prediction predicting a first way of the cache for which

the corresponding value of the plurality of values matches the first value (each array is coupled to receive a portion of a request address, and when data cache receives a requested address, a tag array uses an index portion of the requested address to access a particular set of tags, which are conveyed to a tag comparator, which receives a second portion of the requested address to compare with the selected set of tags; if one of the tags compares equal, there is a "hit" in the cache, and if none of the tags equal the second portion of the address, there is a "miss", col. 13, lines 10-20).

For claim 3, Tran discloses the circuit, if none of the plurality of values matches the first value, is configured to assert an early miss signal (the data cache is pipelined so that the next access is started before the validity of the previous way prediction is determined, col. 15, lines 31-40).

For claim 4, Tran discloses each of the plurality of values comprises a portion of a tag identifying a corresponding cache line in the cache, the portion excluding at least one bit of the tag (col. 3, lines 22-24; col. 13, lines 10-20; a cache line is read and output by the sense amp unit, if the requested address hits in the tag cache, the way prediction is verified by comparator which receives the way prediction after it is selected from way prediction array, col. 14, lines 34-39; offset bits from a request address are used to selected the requested bytes from the cache line, col. 14, lines 35-36).

For claim 5, Tran discloses each of the plurality of values is derived from at least a portion of the indication of the address identifying a corresponding cache line (col. 3, lines 22-24; col. 13, lines 10-20).

For claim 6, Tran discloses each of the plurality of values comprises a portion of one or more address operands used to generate the address (col. 3, lines 22-24; col. 13, lines 10-20).

For claim 7, Tran discloses at least one bit of one of the plurality of values is a logical combination of two or more bits of the address (a first portion of a requested address is used to select a set of way predictions stored within the plurality of storage locations... a first subset of memory locations may be selected based upon a second portion of the requested address and the selected set of way predictions... a second subset of memory locations may be selected based upon the third portion of the requested address... in one embodiment, the second portion and third portion of said requested address may be the same portion of the requested address, col. 3, lines 22-44).

For claim 8, Tran discloses at least one bit of one of the plurality of values is a logical combination of two or more bits of one or more address operands used to generate the address (col. 3, lines 22-44).

For claim 9, Tran discloses the indication of the first address comprises at least a portion of the first address (col. 3, lines 22-24).

For claim 10, Tran discloses the indication of the first address comprises one or more address operands used to generate the first address (col. 3, lines 22-24).

For claim 11, Tran discloses if the way prediction is incorrect, the cache is configured to replace a cache line in the way indicated by the way prediction with a missing cache line corresponding to the first address (if there is no match found in the

tags, a cache miss occurs, and the output data is canceled and the requested data is fetched from main memory, col. 15, lines 31-33).

Claim 13 is rejected using rationale as per rejection of claim 1 above, where Tran discloses both a cache memory and corresponding elements (col. 3, lines 19-67, col. 4, lines 1-4) as well as a method for accessing a cache array and reading a plurality of way predictions from a way prediction array for use with the cache memory and corresponding elements (col. 4, lines 5-24).

Claim 14 is rejected using rationale as per rejection of claims 2 and 13 above.

Claim 15 is rejected using rationale as per rejection of claims 3 and 14 above.

Claim 16 is rejected using rationale as per rejection of claims 4 and 13 above.

Claim 17 is rejected using rationale as per rejection of claims 5 and 13 above.

Claim 18 is rejected using rationale as per rejection of claims 6 and 17 above.

Claim 19 is rejected using rationale as per rejection of claims 7 and 17 above.

Claim 20 is rejected using rationale as per rejection of claims 8 and 17 above.

Claim 21 is rejected using rationale as per rejection of claims 11 and 13 above.

For claim 23, Tran discloses an apparatus comprising:

a way predictor (a cache memory employing way prediction, col. 3, lines 4-5) comprising:

a decoder configured to decode an indication of a first address that is to access a cache, the decoder configured to select a set responsive to the indication of the first address (col. 3, lines 24-29);

a memory coupled to the decoder, wherein the memory is configured to output a plurality of values from a set of storage locations in response to the decoder selecting the set, wherein each of the plurality of values corresponds to a different way of the cache (col. 3, lines 41-44); and

a first circuit coupled to receive the plurality of values and a first value corresponding to the first address, wherein the first circuit is configured to generate a way prediction for the cache responsive to the plurality of values and the first value (col. 3, lines 5-7; col. 3, lines 22-24); and

a data cache data memory coupled to the way predictor, wherein the data cache data memory is arranged into a plurality of ways, and wherein the data cache data memory is configured to output data from a predicted way of the plurality of ways, wherein the predicted way is identified by the way prediction (data cache is a high speed cache memory provided to temporarily store data being transferred between load/store unit and the main memory subsystem, and may employ a way prediction mechanism, col. 10, lines 55-63), and wherein the data cache data memory includes a second circuit configured to reduce power consumption attributable to one or more non-predicted ways of the plurality of ways (die space and power consumption may be reduced through the use of one sense amp unit instead of multiple sense amp units, i.e., one sense amp unit per way or column, col. 3, lines 8-16).

For claim 24, Tran discloses a data cache tag memory configured to output a tag from the predicted way (a tag array uses an index portion of the requested address to access a particular set of tags, which are conveyed to a tag comparator, which receives

a second portion of the requested address to compare with the selected set of tags; if one of the tags compares equal, there is a "hit" in the cache, and if none of the tags equal the second portion of the address, there is a "miss", col. 13, lines 10-20).

Tran does not explicitly disclose not outputting tags from the one or more non-predicted ways, however, this is inherently true in Tran's disclosure. It is only when there is a hit or a correct prediction in the cache that a tag is output and used, therefore a miss or a non-predicted way would inherently not produce a tag to be used.

For claim 25, Tran discloses the second circuit is configured to generate separate wordlines for each of the plurality of ways in the data cache data memory, and wherein the second circuit is configured to activate a first wordline to the predicted way and to not activate word lines to the non-predicted ways responsive to the way prediction (fig. 3, items 50, 52, 54, 56; the data cache comprises a data array of a plurality of memory locations configured into columns, and each column is coupled to a corresponding sense amp unit, each which are coupled to way selection multiplexer and sense amp enable unit, col. 12, lines 20-25).

For claim 26, Tran discloses the second circuit includes column multiplexor circuitry coupled to the plurality of ways and configured to select the output of the predicted way as input to a sense amplifier circuit, wherein the column multiplexor circuitry is controlled by the way prediction (col. 12, lines 20-25).

For claim 27, Tran discloses the second circuit includes column multiplexor circuitry coupled to the plurality of ways and configured to select the output of the

predicted way as input to a sense amplifier circuit, wherein the column multiplexor circuitry is controlled by the way prediction (col. 12, lines 20-25).

For claim 28, Tran discloses the second circuit comprises a plurality of sense amplifier circuits, wherein each of the plurality of sense amplifier circuits is coupled to a respective one of the plurality of ways, and wherein each of the plurality of sense amplifier circuits includes an enable input that is controlled by the way prediction (data from one memory location is then selected for output by way selection multiplexer, which selects a particular column based upon a way prediction read from way prediction array, and the memory location at the intersection of the selected row and column is then read and output, col. 12, lines 39-44).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 12 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tran (US Patent No. 6,016,533) in view of Wickeraad et al (US Patent No. 6,490,654).

For claim 12, Tran fails to disclose if no way prediction is generated and a cache miss results for the first address, the cache is configured to use a replacement algorithm to select the cache line to be replaced with the missing cache line.

Wickeraad discloses a cache memory replacement algorithm that replaces cache lines based on the likelihood that cache lines will not be needed soon (col. 4, lines 50-52).

Tran and Wickeraad are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. Wickeraad suggests that it would have been desirable to incorporate a cache line replacement algorith into the system of Tran because this allows data which is likely needed soon is assigned a higher replacement class, while data that is more speculative and less likely to be needed soon is assigned a lower replacement class (col. 5, lines 2-6). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Tran as suggested by Wickeraad to incorporate the feature as claimed.

Claim 22 is rejected using rationale as per rejection of claims 12 and 21 above.

Citation of Pertinent Prior Art

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Rakvic et al (US PGPub No. 20020188806) discloses parallel cachelets that are independently addressable.

Kavipurapu (US Patent No. 6,584,546) discloses tag portions of an address are compared against sets of tags associated with different sets of data in a cache memory.

Conclusion

When responding to this Office Action:

7. Applicant is requested to indicate where in the disclosure support is to be found for any new language added to the claims by amendment. 37 C.F.R. § 1.75(d)(1) requires such support in the Specification for any new language added to the claims and 37 C.F.R. § 1.83(a) requires support be found in the Drawings for all claimed features.

Applicant must clearly point out the patentable novelty which he or she thinks the claims present, in view of the state of the art disclosed by the references cited or the objections made, and must also explain how the amendments avoid the references or objections. See 37 C.F.R. § 1.111(c).

Contact Information

8. Any inquiries concerning this action or earlier actions from the examiner should be directed to Daniel Kim, reachable at 571-272-2742, on Mon-Fri from 10:00am-6:30pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah, is also reachable at 571-272-4098.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information from published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. All questions

regarding access to the Private PAIR system should be directed to the Electronic Business Center (EBC), reachable at 866-217-9197.

DK

6-10-07

STEPHEN C. ELMORE
PRIMARY EXAMINER